UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

AVAGO TECHNOLOGIES GENERAL IP (SINGAPORE) PTE LTD.,

Plaintiff,

v.

ASUSTEK COMPUTER, INC., et al.,

Defendants.

Case No. 15-cv-04525-EMC

ORDER RE CLAIM CONSTRUCTION

Avago has filed suit against ASUS for infringement of the following patents: the '730, '087, '835, '148, '663, '387, and '830 patents. The parties have asked the Court to construe terms that are contained in five out of the seven patents (*i.e.*, all patents except for the '087 and '387 patents). Below are the Court's constructions.

I. LEGAL STANDARD

Claim construction is a question of law to be determined by the Court. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) ("hold[ing] that in a case tried to a jury, the court has the power and obligation to construe as a matter of law the meaning of language used in the patent claim"). "The purpose of claim construction is to 'determin[e] the meaning and scope of the patent claims asserted to be infringed.'" *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008).

> Words of a claim are generally given their ordinary and customary meaning, which is the meaning a term would have to a person of ordinary skill in the art after reviewing the intrinsic record at the time of the invention. "In some cases, the ordinary meaning of claim language . . . may be readily apparent even to lay judges, and claim construction in such cases involves little more than the

> application of the widely accepted meaning of commonly understood words." However, in many cases, the meaning of a claim term as understood by persons of skill in the art is not readily apparent.

Id.

> Because the meaning of a claim term as understood by persons of skill in the art is often not immediately apparent, and because patentees frequently use terms idiosyncratically, the court looks to "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean." Those sources include "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art."

Phillips v. AWH Corp., 415 F.3d 1303, 1314 (Fed. Cir. 2005). As a general matter, extrinsic evidence such as dictionaries and expert testimony is considered less reliable than intrinsic evidence (*i.e.*, the patent and its prosecution history). *See id.* at 1317-19 (noting that "extrinsic evidence may be useful to the court, but it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence").

Although the specification including embodiments of the claimed invention may be relevant to construction of the claims, generally, such embodiments should not be imported into the claims as limitations. *See Toshiba Corp. v. Imation Corp.*, 681 F.3d 1358, 1369 (Fed. Cir. 2012) ("We do not read limitations from the specification into claims."). "There are only two exceptions to this general rule: (1) when a patentee sets out a definition and acts as his own lexicographer, or (2) when the patentee disavows the full scope of the claim term either in the specification or during prosecution." *Thorner v. Sony Computer Entm't Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012).

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II. '730 PATENT

"first header"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction**
A data structure on a music chip which includes information relating to the way the music tracks were encoded in the memory of the music chip for use by the audio player in decoding the stored music.	A single data structure that contains information corresponding to the way in which pre-recorded audio tracks are encoded for storage in memory, which is used by the audio player to decode tracks for playback.	A single data structure that includes information used by the audio player to decode the collection of individual tracks of audio stored in memory [*i.e.*, the *B&N* construction].

The disputed term for the '730 patent is "first header." That term appears in, *inter alia*, claim 1 which provides as follows:

> **1.** A data format for use in an audio system wherein pre-recorded music is digitally encoded in memory of an integrated circuit music chip, and said music is decoded and reproduced by means of an associated audio player, said data format for storing information pertaining to the contents of said music chip, wherein individual tracks of audio are stored in designated locations in said music chip, said data format including:
>
> **first header** having parameters stored therein for use by said audio player in decoding said digitally encoded music stored in said memory; and
>
> at least one second header, said second header including selectable categorical information relating to said individual tracks of audio stored in said memory.

'730 patent, claim 1 (emphasis added).

Notably, the term "first header" appears for the first time in the claims of the patent. In the specification, the term "global header" is used, but not "first header."

The parties' basic dispute with respect to "first header" is whether it is a *single* data

structure – *i.e.*, "whether there can only be a single 'first header'" as opposed to multiple first headers. Resp. Br. at 1 (emphasis omitted). The parties agree that a global header, as that term is used in the patent, comprises a single data structure, *see* Resp. Br. at 2, but Avago argues that a first header is different from a global header, while ASUS takes the position that the two are the same. (While the term "first header" appears in independent claim 1, "global header" appears in independent claims 18 and 31.)

In *Barnes & Noble, Inc. v. LSI Corp.*, No. C-11-2709 EMC ("*B&N*"), this Court previously construed "first header" to mean the same thing as "global header" and further construed each term as comprising a single data structure. *See* Holohan Decl., Ex. H (Order at 4) (defining "first header" and "global header" in the same way – *i.e.*, as "'a single data structure that includes information used by the audio player to decode the collection of individual tracks of audio stored in memory'"). In *Sandisk v. LSI Corp.*, No. C 09-02737 WHA, 2010 U.S. Dist. LEXIS 24973 (N.D. Cal. Mar. 17, 2010), Judge Alsup in construing the same claim determined that "'first header' is entitled to a broader construction than 'global header'" but nevertheless still agreed with the accused infringer that "there can only be a *single* 'first header.'" *Id.* at *10 (emphasis in original).

Avago acknowledges the above cases such but argues, in effect, that the Court should reconsider its decision and construe the term as another federal court in Texas did. *See* Mot. at 5 n.7 (citing *Agere Sys v. Sony Corp.*, No. 2:06-CV-079, 2008 U.S. Dist. LEXIS 39605, at *45-46 (E.D. Tex. May 15, 2008) (construing "first header" and "global header" differently; finding the latter "a more restrictive term")).

In *B&N*, this Court already considered both *Sandisk* and *Agere*. It ultimately found that the term "first header" must mean a single data structure for the following reasons. (In *B&N*, LSI (Avago's predecessor) argued that *neither* "global header" nor "first header" should be limited to a single data structure.)

> Beginning with the language of the patent, claim 1 and claim 18 speak of a "first header . . . [and] *at least one* second header" and a "global header . . . [and] *at least one* individual header," respectively. '730 Patent, claim 1, 18 (emphases added). *See also*

Interactive Gift Exp., Inc. v. Compuserve Inc., 256 F.3d 1323, 1331 (Fed. Cir. 2001) ("In construing claims, the analytical focus must begin and remain centered on the language of the claims themselves . . . ."). Accordingly, whereas the patent expressly accounts for the existence of more than one individual or second header, the claims – and, in fact, everywhere in the patent – speak of a global or first header in the singular. Thus, the plain text of the claim strongly supports Barnes & Noble's construction. *Sandisk*, 2010 WL 986992, at *4.

Similarly, as the *Sandisk* court recognized, the purpose of the "first header" and "global header" supports the limitation of both terms to a "single data structure." The specification explains that "[t]he present invention is a protocol . . . includ[ing] a *hierarchical* arrangement of headers about selections on the chip and the method in which they were coded." '730 patent, col. 1:48-50 (emphasis added). The hierarchy consists of two tiers: the "global header" (or "first header"), which contains information to "decode the digitally encoded music stored in the memory (e.g., encoding algorithm, bitrate, etc.)," and the "individual header" (or "second header") which contains "information about individual music tracks (e.g., artist, album, genre, etc.)." *Sandisk*, 2010 WL 986992, at *4. The invention summary provides that a "global header located at the very start of memory will specify information needed to successfully decode the content of the music chip" while the individual headers are described as having the "music category to which a track belongs . . . the artist, and information for addressing each track selection." *Id.*, col. 1:51-65; *see also C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 864 (Fed. Cir. 2004) ("Statements that describe the invention as a whole, rather than statements that describe only preferred embodiments, are more likely to support a limiting definition of a claim term."). Accordingly, the Court agrees with the *Sandisk* court that the "weight of intrinsic evidence" demonstrate a "clear intent by the patentee to limit the invention to a hierarchy of headers, where multiple 'music-track-specific' headers corresponded to a single 'decoding' header." *Sandisk*, 2010 WL 986992,at *5.

LSI argues, however, that the patent discloses the possibility of multiple "first" or "global" headers. LSI relies on the declaration of Dr. Jayant who states, in part: "By storing information about the encoding algorithm in the header of a music file (as opposed to having a single file corresponding to an entire memory chip), the patent aimed to make it 'possible to encode more on a single chip using different algorithms . . . [and] at different bit rates.'" Decl. of Dr. Nikil Jayant ("Jayant Decl.") ¶ 13 (Dkt. No. 268-37) (quoting '730 Patent, Col. 2:58-59). However, the specification language upon which Dr. Jayant relies states, in its full context, that:

> The parameter information of the global header **22** is advantageously included because as compression technology evolves, it may be possible to encode more on a single chip using different algorithms, and almost certainly at different bit rates. Thus, rather than 'freeze' the compression algorithm to its current quality using a specific bit rate, it will be more cost

> effective to generate a specific algorithm release for each chip. This would allow an album from a specific artist introduced today to use 128Kbps while an album released at some future date from the same artist could utilize a different algorithm that would play at perhaps 32 Kbps with the same quality that the 128 Kbps piece has at present.

'730 Patent, col. 2:55-67.

While this language is far from a model of clarity, the Court disagrees that this language describes a music chip containing music encoded with differing algorithms or bit rates. Rather, this language recognizes that as compression technology evolves, it "may be possible" to fit more music onto a single chip. This is demonstrated by the "album" example at the end of this passage – the specification speaks of an album released "today" using a 128Kbps bit rate while "at some future date" a more advanced algorithm would allow encoding at a 32Kbps bit rate but at the same quality as a present 128Kbps encoding, but taking up less space in the music chip. *See* Declaration of Dr. Paris Smaragdis ("Smaragdis Decl.") ¶ 8 (Dkt. No. 270-44) ("In other words, while an earlier music chip may encode its music using a particular algorithm, a later music chip may store its music encoded using a different, better algorithm that provides the same quality as the algorithm used in the earlier music chip using a much lower bit rate . . . ."). This passage read in context makes clear that the "different," more advanced, algorithm alluded to in the subject passage pertains to a new algorithm on a new chip, not multiple algorithms on a single existing chip. *See id.* ("Thus, rather than 'freeze' the compression algorithm to its current quality using a specific bit rate, it will be more cost effective to *generate a specific algorithm release for each chip*." (emphasis added)). Accordingly, the Court finds that nothing in the patent discloses having multiple bit rates or algorithms (and thereby requiring a multiplicity of first or global headers) on a single chip.

Finally, although the *Agere* court's holding that "global header" and "first header" should be construed differently – it may be argued that the term "global" more strongly connotes a singular entity with universal application – both parties agree they should be treated similarly, at least on the question of whether they are limited to a "single data structure." The Court notes that the term "first header" only appears in claim 1 and associated dependent claims. It does not appear in the specification, where only "global header" is used to describe the invention as a whole. Significantly, the inventors used the terms interchangeably during the prosecution of the patent. For example, an October 1996 letter sent to a patent examiner states, in part, "[t]he data protocol [described in the patent] contains a global header which will specify information needed to successfully decode the content of the music and at least a second header which is a table of contents that contains various fields of information." Dkt. No. 270-32, at 11. In support of this statement, the inventor cited to claims 1, 18, and 31 – despite the fact that the term "global header" appears nowhere within claim 1.

> The Court is cognizant of the general presumption that different terms were intended to have different meanings. *See Applied Medical Resources Corp. v. U.S. Surgical Corp.*, 448 F.3d 1324 (Fed. Cir. 2006). However, this presumption only exists in the absence of evidence to the contrary. *Id.* Additionally, the Federal Circuit has recognized claim drafters can, and do, use different terms to define the same subject matter – particularly where independent claims are involved. *See Curtiss-Wright Flow Control Corp. v. Velan, Inc.*, 438 F.3d 1374, 1380 (Fed. Cir. 2006) ("Different claims with different words can . . . define different subject matter within the ambit of the invention. On the other hand, claim drafters can also use different terms to define the exact same subject matter."); *Mycogen Plant Science v. Monsanto Co.*, 243 F.3d 1316, 1329 (Fed. Cir. 2001) (citation omitted) ("It is not unusual that separate claims may define the invention using different terminology, especially where . . . independent claims are involved.").
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> Accordingly, the Court finds that both the "first header" and "global header" identified in the '730 patent are limited to a "single data structure." The Court thus provides the following construction for both terms: "a single data structure that contains information corresponding to the way in which pre-recorded audio tracks are encoded for storage in memory, which is used by the audio player to decode tracks for playback."

Holohan Decl., Ex. H (Order at 6-9).

Nothing in Avago's papers alters the Court's analysis above. Avago cites to *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351 (Fed. Cir. 2000), where the Federal Circuit stated that

> an indefinite article "a" or "an" in patent parlance carries the meaning of "one or more" in open-ended claims containing the transitional phrase "comprising."[1] Unless the claim is specific as to the number of elements, the article "a" receives a singular interpretation only in rare circumstances when the patentee evinces a clear intent to so limit the article. Under this conventional rule, the claim limitation "a," without more, requires at least one.

Id. at 1356. But here claim 1 of the '730 patent does not use the word "a" in conjunction with the term "first header." Claim 1 provides as follows:

> **1.** A data format for use in an audio system wherein pre-recorded music is digitally encoded in memory of an integrated circuit music chip, and said music is decoded and reproduced by means of an associated audio player, said data format for storing information

[1] "In the patent claim context the term 'comprising' is well understood to mean 'including but not limited to.'" *Cias, Inc. v. Alliance Gaming Corp.*, 504 F.3d 1356, 1360 (Fed Cir. 2007).

> pertaining to the contents of said music chip, wherein individual tracks of audio are stored in designated locations in said music chip, said data format including:
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> **first header** having parameters stored therein for use by said audio player in decoding said digitally encoded music stored in said memory; and
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> at least one second header, said second header including selectable categorical information relating to said individual tracks of audio stored in said memory.

'730 patent, claim 1 (emphasis added). Thus, *no* article was used at all for "first header." *See also* '730 patent, claim 18 (also using no article for "global header").[2] Moreover, even if the indefinite article "a" had been used, *KCJ* simply states that a singular interpretation is applied "when the patentee evinces a clear intent to so limit the article." *KCJ*, 223 F.3d at 1356. Here, there is such an intent as indicated by the Court's conclusion that the presumption that different terms have different meanings has been overcome.

Nor does the prosecution history create ambiguity as Avago argues. Avago points, for instance, to a statement in the prosecutor history that the "invention primarily deals with a data protocol consisting of a global header or first header containing various information such as algorithm, bit rate, distributor of music, label, and copyright and at least another header containing a preamble, category, artist, and address." Holohan Decl., Ex. I (Amendment at 10). This statement does not clearly treat global header and first header as different things. In fact, one could interpret that statement to mean that global header and first header are the same things – *i.e.*, the use of the term "or" signifies that the two are the same rather than different. Furthermore, that same statement lends support to the construction that a first header must be a single data structure because why would there be multiple first headers (Avago's position) *all* containing information on the distributor of music, label, and copyright? *Cf. Sandisk*, 2010 U.S. Dist. LEXIS 24973, at *14 (noting that, "in a response to a USPTO office action dated June 17, 1996, the patent holder described the 'first header' as containing 'algorithm, bit rate, distributor of music, label, and

[2] Of course, claim 31 of the '730 patent does describe a "method comprising the steps of: storing in *a* global header parameters corresponding to encoding techniques used in storing said pre-recorded audio in memory." '730 patent, claim 31 (emphasis added). However, Avago has conceded that "global header" is a single data structure.

copyright' information," but, "[i]f the patentee truly intended the 'first header' to be used as a 'frame header' in an MP3 bitstream, the patentee would not have described the first header as containing information pertaining to the distributor of music, label, or copyright [as] [s]uch information would have served no purpose in thousands of frame headers within a single music track").

Accordingly, the Court adopts the construction for "first header" that it did in *B&N – i.e.*, "a single data structure that includes information used by the audio player to decode the collection of individual tracks of audio stored in memory."

III. '148 PATENT

The disputed terms for the '148 patent are (1) "synchronisation signal" and (2) "modulating"/"demodulating." Those terms appear in, *inter alia*, claims 8 and 14 which provide as follows:

> **8.** An apparatus for use in an OFDM communication system, the apparatus comprising a first OFDM device for communicating with a second remote OFDM device at a remote station, the first OFDM configured to (i) add a **synchronisation signal** to a plurality of data signals, (ii) generate a plurality of sub-carrier signals in response to **modulating** the synchronisation signal and the data signals, and (iii) generate a plurality of sub-carrier frequency signals in response to an inverse fast fourier transformation of the sub-carrier signals for transmission to the remote station.
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> . . . .
>
> **14.** An apparatus for use in a communication system, the apparatus comprising a first OFDM device for communicating with a second remote OFDM device at a remote station, the first OFDM device configured to (i) generate a plurality of sub-channel signals in response to a fast fourier transformation of a plurality of sub-channel frequency signals received from the second OFDM device, (ii) generate a **synchronisation signal** and a plurality of data signals in response to **demodulating** the sub-carrier signals, and (iii) synchronize a clock to the synchronisation signal.

'148 patent, claims 8, 14 (emphasis added). Claims 8 and 14 combined, in essence, create claim 1.

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A. First Disputed Term

"synchronisation signal"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction**
A signal added to a plurality of data signals prior to modulation to achieve or maintain at least frequency and timing synchronism.	A burst at a predetermined frequency, or a synchronisation code or symbol from which synchronisation information can be derived.	A signal to achieve or maintain frequency and timing synchronism.

The parties have three disputes with respect to the term "synchronisation signal": (1) whether the synchronisation signal must be added to the plurality of data signals prior to modulation; (2) whether the synchronisation signal must achieve or maintain both frequency and timing synchronism; and (3) whether synchronisation signal should be defined by the type of synchronisation it achieves or maintains or by describing what the synchronisation signal is.

On the first issue, Avago argues that the synchronisation signal must be added to the plurality of data signals prior to modulation, while ASUS argues that there is no such requirement. ASUS has the better position. As ASUS points out, Avago's construction of synchronisation signal makes sense with respect to claim 8, which provides that "the first OFDM [is] configured to (i) add a synchronisation signal to a plurality of data signals" and then "(ii) generate a plurality of sub-carrier signals in response to modulating the synchronisation signal and the data signals." '148 patent, claim 8; *see also* Holohan Decl., Ex. L (Lyon Depo. at 15) (ASUS's expert, testifying that he does not dispute that *claim 8* requires the synchronisation signal to be added to the data signals prior to modulation as "[i]t's in the plain language of the claim"). But the construction makes little to no sense with respect to, *e.g.*, claim 14 which talks about a synchronisation signal in a different context (in particular, demodulation): "[T]he first OFDM device [is] configured to (i) generate a plurality of sub-channel signals in response to a fast fourier transformation of a

plurality of sub-channel frequency signals received from the second OFDM device" and then "(ii) generate a synchronisation signal and a plurality of data signals in response to demodulating the sub-carrier signals." '148 patent, claim 14; *see also* Resp. Br. at 5 (noting that "[i]ndependent claim 14 . . . focuses on the receiving end of the OFDM communication system and does not require that a synchronisation signal be added to a plurality of data signals, nor does it require a modulation step").

In its reply brief, Avago argues that

> Claim 14 is a mirror image of Claim 8, and the "synchronisation signal" that is received in Claim 14 is the same synchronisation signal that is transmitted by a transmitter per claim 8. This is clear from Claim 1, which claims a system comprising a device that practices Claim 8 *and* a device that practices Claim 14. Thus, in order to maintain a consistent definition of "synchronisation signal" across the claims, the synchronisation signal in all claims should be construed to have been added to a plurality of data signals prior to a modulation step.

Reply at 3 (emphasis added). But this argument is problematic. Claim 14 is independent of claim 8, as well as claim 1. Avago invokes the general principle that a "claim term should be construed consistently with its appearance in other places in the same claim or in other claims of the same patent," *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342 (Fed. Cir. 2001), but that principle is not dispositive here. A synchronisation signal can be consistently interpreted across the claims as something that reduces interference between OFDM transmissions. That does not mean that synchronisation signal as used in the specific context of claim 14 necessarily incorporates how that term is used in the specific contexts of claims 1 and 8, especially as they are all independent claims *and* there is nothing in the specification to suggest otherwise.

Moreover, even if the Court were to take guidance from claim 8, Avago fails to explain why synchronisation signal as used in claim 8 should be defined as "a signal added to a plurality of data signals prior to modulation" given that other language in claim 8 already conveys the "prior to modulation" concept. *See* '148 patent, claim 8 (discussing the following steps: "(i) add a synchronisation signal to a plurality of data signals, (ii) generate a plurality of sub-carrier signals *in response to modulating* the synchronisation signal and the data signals") (emphasis added). In

other words, to include the "prior to modulation" concept as part of the definition of "synchronisation signal" would be repetitive. *See Asetek Holdings, Inc. v. Coolit Sys.*, No. C-13-0457 JST, 2013 U.S. Dist. LEXIS 170488, at *13 (N.D. Cal. Dec. 3, 2013) (finding proposed limitation "unnecessary as it is largely redundant of surrounding claim language").

The second and third issues – *i.e.*, whether the synchronisation signal must achieve or maintain both frequency and timing synchronism, and whether synchronisation signal should be defined by the type of synchronisation it achieves or maintains or by describing what the synchronisation signal is – are related.

The Court agrees with Avago that there does not appear to be any dispute between the parties about what a synchronisation signal is, and therefore ASUS's proposed construction is of no real benefit. The remaining question is whether a synchronisation signal must achieve or maintain *both* frequency and timing synchronism, and "not just one or the other as ASUS claims." Op. Br. at 11.

It is clear from the '148 patent that the *preferred embodiment* of the invention claimed has a synchronisation signal achieving both frequency and timing synchronism. In the section titled "Description of Preferred Embodiments," there is the following statement: "Particularly important advantages can be obtained by synchronising the slave modem **12** to the master modem **10** both in terms of frequency generation and timing." '148 patent, col. 9:12-14. But that does not necessarily mean that a synchronisation signal is required to achieve/maintain both. A preferred embodiment is simply one representation of the invention claimed. As noted above, an embodiment in the specifications generally should not be read as a limitation on a claim.

That being said, the Court agrees with Avago that, implicitly, the invention claimed must involve both frequency and timing synchronism or else there would be no true orthogonality (*i.e.*, independence) and that would then lead to interference problems. *See* Op. Br. at 10-11 (taking note of phrases used in the patent such as "true orthogonality" and "overall synchronisation"); *see also* Holohan Decl., Ex. N (Katti Depo. at 89) (Avago's expert indicating that, if orthogonality across sub-carriers was desired, then synchronisation of just frequency would not be enough; "a synchronization signal has to help correct both timing and frequency offsets"). The fact that

Avago's expert, Sachi Katti,[3] has never encountered a design that has just, *e.g.*, frequency synchronism, *see* Holohan Depo., Ex. N (Katti Depo. at 88), also indicates that one skilled in the art would understand a synchronisation signal to cover both frequency and timing synchronism.

ASUS protests that there is language in the specification indicating that a synchronisation signal can address solely frequency synchronism or solely timing synchronism. More specifically, in the section titled "Summary of the Invention," there is the following statement.

> Preferably, the synchronisation signal is derived from the frequency used by the first OFDM device, or the first OFDM device is also frequency synchronized to the synchronisation signal.
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> The frequency synchronisation signal may, for example, comprise a burst at a predetermined frequency, or a synchronisation code or symbol from which synchronisation information can be derived.
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> *The frequency synchronisation signal may also represent timing information useable at the second station to time synchronise the second station to the first station.* For example, the timing information may comprise the leading, or trailing, edge of the burst signal, and define a precise reference point in time relative to transmission of OFDM "symbols." In the case of a synchronisation code, synchronisation can be monitored by detecting the energy from the FFT circuit; the energy will be a maximum when receiver is correctly time synchronized.
>
> With this aspect of the invention, it is possible to reduce the effects of design and operating tolerances which might normally cause slight differences in the timing or frequency associated with each independent OFDM device. Such small variations would normally tend to reduce the true orthogonality of the different sub-carriers generated or used by the different OFDM devices, and hence product a degree of interference between the sub-carriers. By improving the overall synchronisation, a high degree of orthogonality can be attained, leading to improved isolation between the transmission and reception sub-carriers.

'148 patent, col. 3:44-4:5 (emphasis added).

The italicized language above, however, does not convey that a synchronisation signal can accomplish *only* timing synchronization without frequency synchronization. It merely states that there is one way (*i.e.*, as part of the frequency synchronisation signal) in which timing synchronization may be achieved. Moreover, the excerpt above actually indicates that the

[3] Dr. Katti is a professor of electrical engineering and computer science at Stanford. *See* Holohan Decl., Ex. N (Katti Depo. at 7).

invention claimed should involve both frequency and timing synchronization in order to achieve "true orthgonality."

The Court thus construes "synchronisation signal" without referring to whether it is added to data signals prior to modulation, and without referencing what it is as opposed to what it is designed to achieve/maintain. In terms of what a synchronisation signal is designed to achieve, the Court construes the term as follows: "a signal to achieve or maintain frequency and timing synchronism."

B. Second Disputed Term

"modulating"/"demodulating"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction (TBD)**
Modulating: Varying some characteristic of the subcarrier waves to be produced at a later time, such as their amplitudes or phases, as the synchronisation signal and the data signals vary. Demodulating: The reverse of modulating.	Modulating: Varying some characteristic of a carrier wave, *e.g.*, the amplitude, frequency, or phase of the wave. Demodulating: Extracting signals from a carrier wave. The reverse of modulating.	Modulating: Varying some characteristic of the subcarrier waves (*e.g.*, amplitude, frequency, or phase), with the waves having those characteristics to be produced at a later time. Demodulating: The reverse of modulating.

The parties do not really disagree that modulation generally relates to varying the characteristic of a carrier wave. However, Avago takes the position that modulation is, in essence, deciding what the characteristics of the wave will be; the actual generation of the physical wave can come later. *See, e.g.*, Op. Br. at 13 (stating that "modulators map data signals and synchronisation signals on . . . a 'constellation'" and that the "constellation points correspond to

analog wave aspects, such as phase and amplitude[;] [t]he mapping at the modulation step sets certain characteristics of the analog wave that will transmit the data"); Reply at 6 (asserting that "the characteristics of the carrier wave are established prior to the IFFT, but a wave having those characteristics is generated at a later time").

Avago's position is supported by the specification. For example, the specification provides that "output is inputted to N_1 channels of a multi-channel modulator **32** for encoding the signal into N1 sub-channels." '148 patent, col. 6:24-26. Thus, the modulator simply encodes; it does not produce a physical carrier wave. Indeed, the specification notes that a digital-to-analog converter does the latter job (*i.e.*, producing the actual physical analogue wave). *See* '148 patent, col. 6:49-52 (noting that "[t]he output from the circuit **38** is fed into a digital-to-analogue converter (DAC) **40** to convert the signals to analogue form for transmission to the communication line **14**").

In its papers, ASUS argues that modulation cannot simply be the mapping described by Avago. ASUS takes this position based, in large part, on the prosecution history for the '148 patent. More specifically, during the prosecution of the '148 patent, the patent holder took the position that the Saeki patent was not invalidating prior art because "Saeki does not disclose or suggest performing the modulation before the IFFT as presently claimed." Lee Decl., Ex. 8 (Amendment at 23-24). ASUS suggests that, if modulation is understood simply to be mapping, then, even in Saeki, mapping actually occurs before the IFFT. *See* Resp. Br. at 11 (arguing that, in Saeki, "[t]he serial to parallel converter 10 and the source banks 12 and 14 map incoming data signals into points in a 'constellation'" but actual modulation of the amplitude and phase of the carrier wave "does not occur until the QAM modulator 26 operates on the signals after they are operated on by the IFFT 16").

The Court is not persuaded. As the Court reads the prosecution history, the patent holder for the '148 patent was simply making note of the different placement of the modulator in Saeki – *i.e.*, after the IFFT, *see* Lee Decl., Ex. 9 (Saeki patent, FIGS. **4A**-**4B**) – which was in contrast to the '148 patent, which had the modulator placed before the IFFT. *See* '148 patent, FIG. **3**. That is undisputedly true. Moreover, the whole process contemplated by the Saeki patent establishes a

different "order" compared to the process contemplated by the '148 patent. For example, in Saeki, the order is IFFT, digital-to-analog conversion, then the modulator. In contrast, in the '148 patent, the order is modulator, IFFT, and only later digital-to-analog conversion. Thus, Avago's position that, for the '148 patent, the actual generation of the physical carrier wave (as indicated in the '148 patent, an analogue wave produced by the digital-to-analogue converter) does not come until after modulation (mapping) is correct. Saeki contemplates a different process – *i.e.*, there is digital-to-analog conversion and then the wave is actually modulated, or changed.

Accordingly, the Court largely adopts Avago's construction, but it modifies the construction to reflect that it is the physical carrier wave that is generated later.

IV. '663 PATENT

A. First Disputed Term

"setting said index value to a threshold"/"set an index value to a threshold"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction**
Plan and ordinary meaning; no construction necessary. Alternatively, setting said index value to a point beyond which there is a change in the manner a program/circuit executes.	Setting said index value to an initial predetermined number.	Setting said index value to a predetermined number.

The first disputed term for the '663 patent is "setting said index value to a threshold"/"set an index value to a threshold." Claim 1 is a representative claim and provides as follows:

> **1.** A method for generating an index value from a codeword for digital video decoding, comprising the steps of:

> (A) **setting said index value to a threshold** in response to a first portion of said codeword having a first pattern;
>
> (B) adding an offset to said index value based on a second pattern in a second portion of said codeword following said first portion in response to said first portion having said first pattern; and
>
> (C) adding a value to said index value based on a third pattern in a third portion of said codeword following said second portion in response to said first portion having said first pattern.

'663 patent, claim 1 (emphasis added).

The Court takes into account that Claim 1 has to do with decoding. The "flip" side – *i.e.*, encoding – is captured by, *inter alia*, claim 12, which provides as follows:

> **12.** A method for generating a codeword from an index value for digital video encoding, comprising the steps of:
>
> (A) generating a first pattern in a first portion of said codeword in response to said index value being at least as great as a threshold;
>
> (B) generating a second pattern in a second portion of said codeword following said first portion representing an offset of said index value above said threshold; and
>
> (C) generating a third pattern in a third portion of said codeword following said second portion representing a value of said index value above said offset.

'663 patent, claim 12. Claim 12, of course, does not use the specific term to be construed – "setting said index value to a threshold" – although it does use a word included therein, *i.e.*, "threshold."

ASUS's proposed construction is the construction that the Court gave to the term in *B&N*. *See* Opp'n at 13; *see also* Holohan Decl. Ex. H (Order at 50). Avago is critical of Avago's construction/the Court's previous construction because it "fails to capture the essence of a 'threshold' – that something changes once you go beyond the 'threshold'" – and "focuses instead on a tangential characteristic that a 'threshold' is known in advance for a given codeword type." Reply at 9. Avago also contends that the use of the term "predetermined" – although technically correct[4] – is vague and confusing: to the extent it "implies that the sub-term 'threshold' is constant

[4] At the hearing, Avago conceded that a threshold is predetermined in advance of decoding or encoding.

across all codeword types, this is contradicted by the specification which shows that the claimed 'threshold' varies depending on the type of codeword being assessed." Reply at 9. Finally, Avago asserts that the use of the term "initial" is also confusing because "the full disputed terms above are found only in Claims 1 and 11 – both decoding claims":

> Calling the "threshold" an "initial" number, while unnecessary, at least makes some sense in the context of Claims 1 and 11 when "setting said index value to a threshold" during decoding. Asserted Claims 12 and 21, however, are encoding claims. In those claims, no value is ever set to a "threshold." Instead, the sub-term "threshold" is only used as an inflection point beyond which the encoding protocol changes from generating a first pattern to generating a second pattern.

Reply at 9 (emphasis omitted).

Avago's first two arguments are not persuasive. For example, the concept of change is adequately conveyed when the claim is read as a whole. Also, the term "predetermined" does not, in and of itself, suggest that the threshold is constant across all codewords, and there is no danger that ASUS might try to argue such given that, at the hearing, it stated that it would not. Finally, the concept of "predetermined" is not, as suggested by Avago at the hearing, implicit in the term "threshold." Rather, the Court agrees with ASUS that, in principal, there can be a threshold without that threshold being known in advance.

The Court, however, does find merit to Avago's final argument. Although the Court is technically construing the entire term "setting said index value to a threshold," ASUS's construction boils down to defining "threshold" (*i.e.*, because the construction repeats the phrase "setting said index value to"). There could be some confusion if the Court were to use the word "initial" in defining "threshold" because the term "threshold" is repeated in Claim 12. Accordingly, the Court hereby adopts the following construction for the term "setting said index value to a threshold": setting said index value to a predetermined number.

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B. Second Disputed Term

[Whether steps of the method must be performed in order]		
Avago's Position	**ASUS's Position**	**Court's Position**
The steps/system elements of the independent claims are not required to be performed or arranged in any order.	The steps defined in Claims 1, 11, 12, and 21 must be performed in order.	The steps defined in Claims 1, 11, 12, and 21 must be performed in order.

The independent claims at issue in this litigation are claims 1, 11, 23, and 21. The dispute between the parties regarding these claims are whether the steps identified therein must be performed in order, *i.e.*, in a sequence. ASUS argues that ordering is required; Avago argues to the contrary.

As a preliminary matter, the Court takes note that claims 11 and 21 are system claims while claims 1 and 12 are method claims. Avago contends that ASUS's "order" argument applies only to the method claims, not the system claims, because Federal Circuit law has purportedly recognized ordering only with respect to the former, not the latter. *See, e.g., Kaneka Corp. v. Xiamen Kingdomway Grp. Co.*, 790 F.3d 1298, 1306 (Fed. Cir. 2015) (stating that, "[w]here the steps of a method claim actually recite an order, we ordinarily construe the claim to require order"; adding that "[a] method claim can also be construed to require that steps be performed in order where the claim implicitly requires order, for example, if the language of a claimed step refers to the completed results of the prior step"); *see also Netflix, Inc. v. Rovi Corp.*, No. 11-cv-6591-PJH, 2015 U.S. Dist. LEXIS 92766, at *13 (N.D. Cal. July 15, 2015) (noting that party failed to point to any "binding authority holding that a system claim can be required to perform steps in a certain order, or to be 'operative to perform' steps in a certain order").

The Court is not persuaded by Avago's argument. Avago has not cited to any Federal Circuit opinion foreclosing consideration of ordering in a system/apparatus claim. In *Oak Tech, Inc. v. ITC*, 248 F.3d 1316 (Fed. Cir. 2001), the Federal Circuit, in fact, took note that the "required interactions, based solely on the plain language of the claim [a system/apparatus claim],

support the Commission's observation that the claim language contemplates and explicitly describes a sequential process." *Id.* at 1325. Several district courts have also concluded that order can be required by a system/apparatus claim. *See, e.g.*, *Motorola Mobility, Inc. v. Microsoft Corp.*, No. C11-1408JLR, 2012 U.S. Dist. LEXIS 191186, at *69-70 (W.D. Wash. June 4, 2012) (stating that "[i]t is proper to import this requirement into a system claim in this instance because the claim language explicitly provides for the sequence, and the claim language reflects the similar steps as the method claim that requires an ordering of steps"); *Gerber Sci. Int'l, Inc. v. Roland DGA Corp.*, No. 3:06-cv-2024 (CFD), 2011 U.S. Dist. LEXIS 57394, at *5 (D. Conn. May 27, 2011) (stating that, "to the extent apparatus claim 16 incorporates language describing the method of claim 1 – which the Court ruled has an order bias – that order bias is incorporated into that apparatus claim"; adding that "those apparatus claims which necessarily describe an ordered method as part of the description of what the apparatus does incorporate an order," and "Roland is correct that 'a claim term cannot be given a different meaning in the various claims of the same patent'"); *FotoMedia Techs., LLC v. AOL, LLC*, No. 2:07-cv-255, 2009 U.S. Dist. LEXIS 62542, at *39 (E.D. Tex. July 21, 2009) (noting that "some systems claims might be read to incorporate a sequential limitation"); *Lextron Sys., Inc. v. Microsoft Corp.*, No. C-04-0588 VRW, 2005 WL 6220089, at *10 (N.D. Cal. June 1, 2005) (stating that, "[a]lthough claim 1 is not strictly a method claim, it recites steps, so Federal Circuit precedent on methods is appropriately invoked here" – *i.e.*, on ordering/sequencing).

Avago argues that, even if ordering can be a part of a system claim, there is no sequenced process in either in its system or method claims. The general rule is that, "although a method claim necessarily recites the steps of the method in a particular order, . . . the claim is not limited to performance of the steps in the order, unless the claim explicitly or implicitly requires a specific order. The specification or prosecution history may also require a narrower, order-specific construction of a method claim in some cases." *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1345 (Fed. Cir. 2008); *see also Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1342 (Fed. Cir. 2001) (stating that, "[u]nless the steps of a method actually recite an order, the steps are not ordinarily construed to require one").

That ordering is required by the patent is made clear through Claim 12. Claim 12 (encoding) provides as follows:

> **12.** A method for generating a codeword from an index value for digital video encoding, comprising the steps of:
>
> (A) generating a first pattern in a first portion of said codeword in response to said index value being at least as great as a threshold;
>
> (B) generating a second pattern in a second portion of said codeword following said first portion representing an offset of said index value above said threshold; and
>
> (C) generating a third pattern in a third portion of said codeword following said second portion representing a value of said index value above said offset.

'663 patent, claim 12. The critical question is whether ordering is required in steps (B) and (C). As ASUS argues, a sequence is clearly contemplated as reflected by the language "following said first portion" and "following said second portion." While Avago contends that this is just positional sequencing (like a puzzle), and not temporal sequencing, the Court does not agree, particularly in light of the additional language in step (C) which refers to "generating a third pattern . . . representing a value of said index value *above said offset*." '663 patent, claim 12 (emphasis added). The "offset" referred to in step (C) is the offset first referenced in step (B). Thus, the offset must first be established in step (B) before an index value above said offset can be established in step (C).

That ordering is required is confirmed by the specification for the '663 patent. For example, the specification includes the following language.

> Referring now to FIG. **4**, a flowchart of a process for codeword construction is shown generally as **100**. Process **100** illustrates the steps of the present invention. Process **100** begins at step **102** where a test is made to determine if the value of the code symbol index is less than the value of the threshold. If it is processing moves to step **104** [where] a unary codeword is constructed comprising a series of v 1's terminated with a 0. Processing then ends at step **112**. Returning to step **102** if the test is negative, processing moves to step **106**, *where an initial prefix of N 1's is created*. Processing then moves to step **108** where the most significant bits of the value v – (N – 2) are extracted and converted to a unary representation. The unary representation is then *appended to the initial prefix to create a*

> *unary prefix*. Process **100** then moves to step **110** where the binary representation of the least significant bits of the value of value v – (N – 2) are *appended to the unary prefix to create the codeword*.

'663 patent, col. 6:44-7:13 (emphasis added). The italicized language above reflects steps (A), (B), and (C). Nowhere in the specification is it suggested that order is not a part of the process. *Cf. ICU Med., Inc. v. Alaris Med. Sys.*, 558 F.3d 1368, 1374-75 (Fed. Cir. 2009) (agreeing with district court's construction of "spike" to mean "'an elongated structure having a pointed tip for piercing the seal, which tip may be sharp or slightly rounded'" because it is "appropriate 'to rely heavily on the written description for guidance as to the meaning of the claims'" and "the specification 'repeatedly and uniformly describes the spike as appointed instrument for the purpose of piercing a seal inside the valve'").

In its papers, Avago does not really address claim 12, simply asserting that the "order of steps in Claim 12 is immaterial to any infringement issue" and that the focus should be on claim 1 instead. Reply at 10. But it is not clear how Avago can brush off claim 12 given that it is one of the claims allegedly infringed. Moreover, Avago does not dispute that claims 1 and 12, although independent, are flip sides of one another; thus, if order is required for claim 12 (encoding) then the same is implicitly required for claim 1 (decoding), *especially* as the text of the specification expressly indicates that claim 1/decoding is simply a reversal of claim 12/encoding. *See also* '663 patent, col. 4:13-23 (in describing decoding process, noting that the inverse binarization module **72** "reverses the binarization of module **62** (see FIG. **2**)").

Accordingly, the Court concludes that ordering is required for both the system and method claims at issue.

V. '830 PATENT

"synchronization code(s)"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction**
Plain and ordinary meaning; no construction necessary.	This term is indefinite.	The term is not indefinite.

"Synchronization code(s)" appears in, *inter alia*, claim 5 of the '830 patent. Claim 5 provides as follows:

> **5.** A system for synchronizing a data processing unit to a bitstream having successively spaced **synchronization codes** and data disposed between **the synchronization codes**, the bitstream further comprising a data header following each **synchronization code** including information from which intervals between successive **synchronization codes** can be calculated, the system comprising:
>
> a detector for detecting said **synchronization codes**;
>
> a sensor for sensing intervals between successive **synchronization codes**;
>
> a comparator for comparing said intervals with **synchronization code** intervals.;
>
> a controller for determining if the system is synchronized to the bitstream depending on satisfaction of a first predetermined condition and if the system is unsynchronized to the bitstream depending on satisfaction of a second predetermined condition; and
>
> a sensor for sensing said data header and calculating intervals between **successive synchronization codes** from said information.

'830 patent, claim 5 (emphasis added).

As indicated above, the parties' dispute regarding "synchronization code(s)" has to do with whether that term is indefinite.[5]

"The definiteness requirement is set forth in 35 U.S.C. § 112 . . . , which states that '[t]he specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.'" *DDR Holdings, LLC v. Hotels.com, L.P.*, 773 F.3d 1245, 1260 (Fed. Cir. 2014). In *Nautilus, Inc. v. Biosig Instruments, Inc.*, 134 S. Ct. 2120 (2014), the Supreme Court held a patent is invalid for indefiniteness if its claims, read in light of the specification and the prosecution history, failed to inform, with reasonable certainty, those skilled in the art about the scope of the invention. *See id.* at 2130. Whether a claim is indefinite or definite is a question of law. *See DDR Holdings*, 773 F.3d at

[5] At the hearing, the parties represented that they no longer had a dispute regarding the '830 term "a detector for detecting said synchronization codes."

1260.

In the instant case, ASUS seems to admit that a synchronization code is, generally speaking, a definite thing. In its brief, for example, it notes that "[t]he 'synchronization code' is a special pattern of 1s and 0s 'used to designate the beginning of a frame of compressed audio data' and may be utilized by the decoder to synchronize to the audio bitstream." Resp. Br. at 16; *see also* Op. Br. at 18-19 (pointing out that the specification even gives a *specific example* of a synchronization code – *i.e.*, "'a very simple 12-bit synchronization code, binary 1111 1111 1111'") (emphasis added). Nevertheless, ASUS still argues that there is an indefiniteness problem because "the independent claims 1, 5, 16, and 20 use the term ['synchronization code] recklessly such that a person of ordinary skill in the art must necessarily guess as to whether it means a *valid* 'synchronization code,' an *invalid* 'synchronization code,' or both." Resp. Br. at 17.

The Court is not persuaded by ASUS's argument. In its reply brief, Avago fairly explains why ASUS's position is meritless:

- First, it is possible to substitute ASUS's definition above – *i.e.*, "a special pattern of 1s and 0s" – into the claims and have the claims make sense. *See* Reply at 13 (using ASUS's definition in claim 5).
- Second, "ASUS has provided exactly zero evidence that a person of ordinary skill in the art would have any difficulty understanding the meaning of the claim term." Reply at 14.
- And finally, "but for the location of the synchronization code in the bitstream, *valid and invalid synchronization codes are identical – i.e.*, the 'special pattern of 1s and 0s' are the same for each. Indeed, the controller limitation that ASUS . . . omitted from its claim chart indicates that the system described in claim 5 is directed at least in part *to determining whether a particular synchronization code is valid or invalid*." Reply at 14 (emphasis added).

Accordingly, the Court rejects ASUS's contention that the term "synchronization code(s)" is indefinite.

VI. '835 PATENT

"navigation data"		
Avago's Proposed Construction	**ASUS's Proposed Construction**	**Court's Construction (TBD)**
Data indicating the physical location of a beginning of a selected portion of a presentation stored upon the optical disk.	Plain meaning, *i.e.*, data indicating the physical location of presentation data on an optical disk.	Data indicating the physical location of presentation data on an optical disk.

The disputed term for the '835 patent is "navigation data." The term appears in, *inter alia*, claim 1 which provides (as corrected)[6] as follows:

> **1.** An optical disk system, comprising:
>
> a disk drive unit for retrieving identification data, encoded video data, and **navigation data** from an optical disk positioned therein, wherein the identification data of the optical disk identifies the optical disk, and wherein the encoded video data comprises a presentation;
>
> an input device configured to produce an output signal in response to user input, wherein the output signal indicates user selection of a portion of the presentation and occurs when a beginning of the user selected portion is currently being played;
>
> a memory unit comprising a non-volatile portion; and
>
> a control unit coupled to receive the identification data and the **navigation data** from the disk drive unit and the output signal produced by the input device, wherein the control unit is coupled to the memory unit, and wherein the control unit responds to the output signal by:
>
> producing the current navigation data, wherein the current navigation data identifies the beginning of the user selected portion of the presentation currently being played; and

[6] There is a certificate of correction for the patent. The certificate should be referred to for the correct claims.

> storing the identification data and the current navigation data within the non-volatile portion of the memory unit such that: (i) the identification data and the current navigation data exist in the non-volatile portion of the memory unit concurrently, and (ii) the current navigation data is associated with the identification data within the non-volatile portion of the memory unit.

'835 patent (emphasis added). As indicated above, claim 1 uses both the term "navigation data" and a more specific term "current navigation data." That claim 1 uses both the term "navigation data" and the separate term "current navigation data" indicates that the two terms have different meanings. *See Augme Techs., Inc. v. Yahoo! Inc.*, 755 F.3d 1326, 1333 (Fed. Cir. 2014) (noting that "'[d]ifferent claim terms are presumed to have different meanings'").

The basic dispute between the parties is whether the term "navigation data" refers to the physical location of presentation data on an optical disk generally (ASUS's position) or to the beginning of *a selected portion* of the presentation specifically (Avago's position). ASUS has the stronger position. While there are some places in the patent that refer to navigation data as "data indicating the physical location of a beginning of a selected portion of a presentation," ('835 patent, abstract), that reference seems to utilize a "loose" use of the term; reading the patent as a whole indicates that it is *current* navigation data specifically (and not navigation data without the modifier "current") that is data indicating the physical location of a beginning of a selected portion of a presentation. For example:

> One embodiment of the optical disk system includes a memory unit operably coupled to a disk drive unit and an input device. The disk drive unit retrieves identification data, encoded video data, and navigation data stored upon an optical disk (e.g., a DVD). The encoded video data may be, for example, a recorded presentation such as a movie.
>
> The input device may include a keypad having multiple electrical pushbutton switches or "keys." A user may cause the input device to produce the output signal by pressing one or more of the keys of the keypad. The occurrence of the output signal may indicate the beginning of a selected portion of the encoded video data (i.e., presentation). When the output signal is received from the input device, the *current* navigation data identifies the physical location of the beginning of the selected portion of the presentation on the optical disk. The *current* navigation data is stored within the memory unit. The stored navigation data is later retrieved and used to locate the encoded video data corresponding to the selected

> portion of the presentation. Retrieval of the stored navigation data corresponding to the selected portion of the presentation allows replay of only the selected portion of the presentation (e.g., a favorite movie scene).
>
> The memory unit includes a non-volatile portion for storing the identification data and the current navigation data. . . .
>
> The data stored within the memory unit may include identification data and index information, wherein the index information includes a navigation data portion and a time index portion. . . .
>
> The navigation data portion identifies the physical location of the beginning of the selected portion of the presentation on the optical disk as describe[d] above.

'835 patent, col. 2:13-66 (emphasis added). In the last paragraph above, the phrase "navigation data portion" – when taken in the above context – clearly refers to current navigation data. Although the phrase does not use the word "current," the whole concept of *selection* is applicable to current navigation data only, as indicated by the paragraphs preceding the last paragraph.

Accordingly, the Court agrees with ASUS that "navigation data" itself (as opposed to current navigation data) simply means "data indicating the physical location of presentation data on an optical disk."

VII. CONCLUSION

For the foregoing reasons, the Court adopts the above constructions.

IT IS SO ORDERED.

Dated: May 27, 2016

EDWARD M. CHEN
United States District Judge